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EXAMINER	
CHAUHAN, LOREN B	
ART UNIT	**PAPER NUMBER**
2193	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/720,096	PALAT ET AL.	
	Examiner	Art Unit	
	Loren Chauhan	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-49* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-49 are pending for examination.

Claim Objections

2. Claims 21 and 39 are objected because of the following informalities: Examiner notes the use of "gcc 2.96" acronyms in above claims. Use of acronyms in claim language should be explained in plain text. Appropriate correction required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-49 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

a. The following terms lack antecedent basis:

i. The instruction pointer – claim 3.

b. The claim language in the following claims are not clearly understood:

ii. As per claim 1, lines 3-4, it is not properly explained who is locating one or more instances (i.e. instruction pointer or instruction offset pointer). Also, it is not clear based on what information locating instances of one or

more data-relative offset in code segment occurs (i.e. based on address instruction pointer). Line 5, it is unclear who is calculating a new offset (i.e. instruction pointer) and based on what information (i.e. based on present data-relative offset). Line 6, it is not specifically explain who is replacing data-relative offset with the new offset (i.e. compiler).

iii. As per claim 25, it is a system claim of claim 1, therefore; it is rejected for the same reason as per claim 1.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-7, 9-10, 12-27, 29-30, 32-41 and 43-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Peterson (US Pat. No. 5,504,901).

7. As per claim 1, Peterson teaches the invention as claimed including a method of enabling execution of data-relative code within a non data-relative environment (Abstract lines 1-5), including the steps of:

i) locating one or more instances of the use of a data-relative offset within a module of a code segment (col. 4, lines 37-42);

ii) calculating a new offset independent of a data segment (col. 7, lines 35-40); and

iii) replacing the data-relative offset with the new offset in the code segment module (col. 7, lines 59-64).

8. As per claim 2, Peterson teaches the invention including the method, wherein the data-relative offset is used for computing the target address of a branch instruction (col. 14, lines 7-10).

9. As per claim 3, Peterson teaches the invention including the method, wherein the new offset is relative to the instruction pointer (col. 9, lines 1-3).

10. As per claim 5, Peterson teaches the method, wherein steps (i) to (iii) occur during runtime of an application using the code segment (col. 9, lines 25-29).

11. As per claim 6, Peterson teaches the method, including the step of:

iv) executing the modified code segment module (col. 12, lines 62-67).

12. As per claim 7, Peterson teaches the method, wherein the code segment module is executed on an HP-UX platform (col. 13, lines 6-10).

13. As per claim 9, Peterson teaches the method, wherein the code segment module is executed on a non-native platform (col. 13, lines 6-10).

14. As per claim 10, Peterson teaches the method, wherein the new offset is an absolute runtime address (col. 12, lines 1-7).

15. As per claim 12, Peterson teaches the method, wherein steps (i) to (iii) occur outside of the runtime of the application using the code segment (col. 6, lines 60-63).

16. As per claim 13, Peterson teaches the method, including the step of: v) saving the modified code segment module to non-volatile memory (fig. 3A; col. 5, lines 25-30).

17. As per claim 14, Peterson teaches the method, wherein the code segment module is within a shared library (col. 18, lines 27-30).

18. As per claim 15, Peterson teaches the method, including the step of: vi) copying the code segment module to modifiable memory (col. 6, lines 60-65); wherein step (vi) occurs before step (iii) and wherein step (iii) the data-relative offset is replaced in the copied code segment module (col. 4, lines 27-30).

19. As per claim 16, Peterson teaches the method, including the step of: vii) allocating the modifiable memory read, write and execute permissions; wherein step (vii) occurs before step (vi) (col. 6, lines 8-13).

20. As per claim 17, Peterson teaches the method, wherein the code segment within the shared library is mapped as writable (col. 19, lines 28-31).

21. As per claim 18, Peterson teaches the method, wherein the code segment module is one selected from the set of an .init section from the shared library and a .fini section from the shared library (col. 18, lines 27-30).

22. As per claim 19, Peterson teaches the method, wherein the code segment is within an application (col. 6, lines 34-36).

23. As per claim 20, Peterson teaches the method, wherein the code segment was compiled using a compiler which inserts code that uses data-relative offsets (46, fig. 1; col. 6, lines 39-41).

24. As per claim 21, Peterson teaches the method, wherein the code segment was compiled using gcc 2.96 (46, fig. 1; col. 6, lines 39-41).

25. As per claim 22, Peterson teaches the method, wherein a dynamic loader performs all the steps (48, fig. 1, col. 6, lines 60-65).

26. As per claim 23, Peterson teaches the method, wherein the data-relative offset is located in step (i) by backtracing the target register of the branch instruction (fig. 4, col. 15, lines 17-23).

27. As per claim 24, Peterson teaches the method, wherein the code segment is a Linux code segment (col. 4, lines 7-9).

28. As per claims 25-27, they are the system claims of claim 1-3, therefore; they are rejected for the same reason as per claims 1-3.

29. As per claims 29-30, they are the system claims of claims 6 and 10, therefore; they are rejected for the same reason as per claims 6 and 10.

30. As per claims 32-35, they are the system claims of claims 13-16, therefore; they are rejected for the same reason as per claims 13-16.

31. As per claims 36-39, they are the system claims of claims 18-21, therefore; they are rejected for the same reason as per claims 18-21.

32. As per claim 40, it is the system claim of claim 24, therefore; it is rejected for the same reason as per claim 24.

33. As per claims 41 and 43, they are the system claims of claims 7 and 9, therefore; they are rejected for the same reason as per claims 7 and 9.

34. As per claim 44, Peterson teaches a code segment module modified by the method (col. 4, lines 7-9).

35. As per claim 45, Peterson teaches a binary file containing a code segment module modified by the method (col. 4, lines 7-9).

36. As per claim 46, Peterson teaches Software for affecting the method (col. 4, lines 7-9).

37. As per claim 47, Peterson teaches Storage media including the software (14, fig. 1).

38. As per claim 48, Peterson teaches a computer system for affecting the method (fig. 1; col. 5, lines 59-60).

39. As per claim 49, Peterson teaches a memory storing the software (14, fig. 1).

Claim Rejections - 35 USC § 103

40. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

41. Claims 4, 11, 28 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson (US Pat. No. 5,504,901).

42. As per claim 4, Peterson teaches the invention substantially including a method, wherein the new offset is calculated using the formula:

new offset = the new offset (col. 10, lines 51-52);

link_time_data_address = the data address during link time (col. 10, lines 53-54);

data_relative_offset = the address relative to the data address (col. 10, lines 55-57);

link_time_module_start = the address of the start of the module of the code segment during link time (col. 11, lines 3-6); and

instruction_pointer_offset = the offset, relative to the start of the code segment module, of the instruction that calculates the new address using the instruction pointer (IP) (col. 11, lines 6-10).

43. However, Peterson does not explicitly teach new offset = link time data address + data relative offset -- (link_time_module_start + instruction_pointer_offset).

44. Peterson teaches a method for mathematically calculating memory field that store the address of the procedure being called is locatable by means of a memory offset pointer value that indicates the memory location of the memory field relative to an instruction of the call sequence (col. 10, lines 42-col. 11 lines 1-15).

45. It would be obvious to one of ordinary skill in the art that the mathematical relationship described in Peterson's system is similar to the applicant's mathematical relationship and can be achieved by mathematical manipulation from Peterson's relationship.

46. As per claim 11, Peterson teaches the method, wherein the absolute runtime address is calculated using the formula: wherein:

runtime_addr = the absolute runtime address (col. 10, lines 51-52);

link_time_data_addr = the data address during link time (col. 10, lines 53-54);

data_relative_offset = the address relative to the data address (col. 10, lines 55-57;

link_time_code_segment_start = the address of the start of the code segment during link time (col. 11, lines 3-6); and

run_time_code_segment_start = the absolute address of the start of the code segment during runtime (col. 11, lines 6-10).

47. Peterson does not explicitly teach runtime addr = link time data addr + data relative offset - link_time_code_segment_start + runtime_code_segment._start.

48. Peterson teaches a method for mathematically calculating memory field that store the address of the procedure being called is locatable by means of a memory offset pointer value that indicates the memory location of the memory field relative to an instruction of the call sequence (col. 10, lines 42-col. 11 lines 1-15).

49. It would be obvious to one of ordinary skill in the art that the mathematical relationship described in Peterson's system is similar to the applicant's mathematical relationship and can be achieved by mathematical manipulation from Peterson's relationship. Also, Peterson's system's processor uses the address stored in the procedure entry point register in execution of called procedure (col. 11, lines 33-35).

50. As per claim 28, it is a system claim of claim 4, therefore; it is rejected for the same reason as per claim 4.

51. As per claim 31, it is a system claim of claim 11, therefore; it is rejected for the same reason as per claim 11.

52. Claims 8 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peterson (US Pat. No. 5,504,901) in view of Lee (US Pat. No. 5,828, 884).

53. As per claims 8 and 42, Peterson does not explicitly teach wherein the code segment is compiled for a little-endian system and the code segment module is executed on a big-endian system.

54. Lee teaches the wherein the code segment is compiled for a little-endian system and the code segment module is executed on a big-endian system (see Byte Swapping Device on col. 7-col. 8).

55. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to combine the teachings of Peterson and Lee because it will improve the system which allows software developers to develop more efficient, portable and bug-free code with respect to byte ordering issues (Lee col. 3, lines 48-50).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Loren Chauhan whose telephone number is 571-270-1554. The examiner can normally be reached on Mon.-Thr. 9:30-5:00 (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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